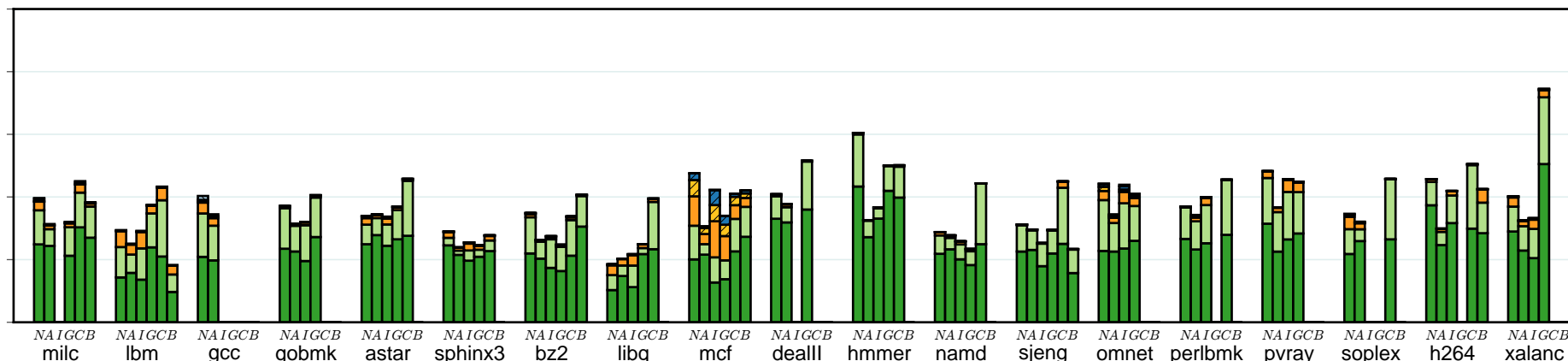


SPEC

Cache hits and misses
(w.r.t. all instructions, %)100
80
60
40
20
0

- L1 load hits
- L1 store hits
- L2 load hits
- ▨ LLC load hits
- ▨ LLC load misses
- ▨ LLC store misses

- N* Native (GCC)
- A* ASan (Clang)
- I* MPX (ICC)
- G* MPX (GCC)
- C* SAFECode (Clang)
- B* SoftBound (Clang)